

WHAT IS CLAIMED IS:

- 1 1. A particularly configurable processor for processing error induced computer
2 programs which are selectively operable on said particularly configurable processor,
3 comprising:
4 a programmable error correcting circuit;
5 an instruction buffer for receiving instructions for microprocessor execution
6 memory location for storing an error correction key; and
7 the error correcting circuit controlled at least in part by said error correction key.
- 1 2. The processor of claim 1, wherein the control of the error correction circuit
2 permits correction in a predictable manner of intentionally inserted errors in a program
3 provided for execution in accordance with an error correction scheme selected.
- 1 3. The processor of claim 1, wherein said key enables selection of error correction
2 specific to the induced error scheme.
- 1 4. The processor of claim 1, wherein information provided in compiled computer
2 program data in part controls said error correction, thereby providing complementary
3 error correction with a combination of the error correction key and the information
4 provided in the compiled computer program data.
- 1 5. The processor of claim 4, wherein the key includes bits expandable into a larger
2 set of bits which control the instruction op code decoder, signal routing, and logic circuit
3 reconfiguration.
- 1 6. The processor of claim 1, wherein a serial number in ROM participates in the
2 control of the programmable error correcting circuit.
- 1 7. The processor of claim 1, wherein an output register for data results is provided,
2 the output register able to contain both correct results and plausible wrong results.
- 1 8. The processor of claim 1, wherein:
2 program instructions are provided in a pipeline architecture;

1 an information key is established as instruction security commands at a plurality of
2 steps in said pipeline architecture; and

3 an arithmetic logic unit (ALU) provides variability of logic circuits for execution
4 of encrypted op codes or standard op codes that provide standard instruction op code
5 operation types.

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9. The processor of claim 8, further comprising:

10 a plurality of reconfigurable logic circuits able to calculate results of execution of
11 an instruction;

12 a plurality of logic circuits including provisions for accepting correct data
13 operands and plausible wrong data operands; and

14 said plurality of the logic circuits including provisions for outputting correct
15 results along with plausible wrong results.

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19. The processor of claim 8, further comprising:

20 the key providing a capability of re-allocating memory resources and register
21 resources;

22 a serial number in ROM which participates in the allocation of logic circuits and
23 routing of signals; and

24 the serial number used in combination with the key in providing said capability.

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28. The processor of claim 1, wherein:

29 instruction key information is shared with a compiler, the instruction key
30 information used by the compiler to encrypt standard instruction op codes into encrypted
31 instruction op codes; and

32 the key is stored in more than one memory cell type including a Read Only
33 Memory (ROM), an Electrically Erasable Programmable Read Only Memory (E²PROM),
34 and a Random Access Memory (RAM).

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38. The processor of claim 1, wherein:

39 an output register for data results provides a capability of providing data
40 containing both correct results and plausible wrong results; and

1 the correct results are provided in word locations in the output register coordinated
2 by the key.

1 13. The processor of claim 1, wherein data and instructions provided to a computer
2 via program information include an intentional introduction of errors which are
3 correctable with error correction algorithms, said correction algorithms pre-selected
4 according to the key.

1 14. The processor of claim 1, wherein:
2 dependency validation codes received through the multiplexer of the instruction
3 buffer are checked by logic circuits that depend on the key, so that incorrect validation
4 bits provide an alarm.

1 15. The processor of claim 14, wherein:
2 upon receipt of said alarm, the interdependency checking logic writes an audit
3 code and is capable of terminating program execution.

1 16. The processor of claim 1, further comprising:
2 logic for requiring network handshaking, the network handshaking further used to
3 provide additional key information for continued operation.

1 17. A microprocessor for processing computer programs which are selectively
2 operable on selected ones of individual microprocessors, comprising:
3 an error correcting circuit;
4 a programmable feature on the error correcting circuit, providing a selectability in
5 an error correction scheme to be performed by the error correcting circuit; and
6 a memory location for storing error correction information, whereby the stored
7 error correction information controls the programmable feature, thereby permitting
8 correction of intentionally inserted errors in a program provided for execution in
9 accordance with an error correction scheme selected.

1 18. Method for processing computer programs selectively operable on one or more
2 selected individual microprocessors, comprising:
3 providing an error correcting circuit;
4 storing error correction control information in the form of an error correction key,
5 thereby selecting an error correction scheme for execution in accordance with the key;
6 and
7 compiling program instructions in accordance with the selected error correction
8 scheme, thereby permitting correction in a predictable manner of intentionally inserted
9 errors in a program provided for execution in accordance with the error correction
10 scheme selected.

1 19. The method of claim 18, further comprising:
2 controlling said error correction controlled in part by information provided in
3 compiled computer program data, thereby providing predictable error correction with a
4 combination of the error correction key and the information provided in the compiled
5 computer program data.

1 20. The method of claim 18, further comprising:
2 using reconfigurable logic circuits for calculating the results of execution of an
3 instruction op code;
4 the calculation of results of the execution of an instruction op code including
5 accepting correct data operands and plausible wrong data operands; and
6 outputting correct results along with plausible wrong results.

1 21. The method of claim 18, further comprising:
2 providing program instructions in a pipeline architecture; and
3 establishing information keys as instruction security commands at a plurality of
4 steps in said pipeline architecture, wherein an arithmetic logic unit (ALU) provides
5 variability of logic circuits for execution of encrypted op codes or standard op codes that
6 provide standard instruction operation types.

1 22. The method of claim 18, further comprising:
2 providing a key shared with a compiler;
3 encrypting standard instructions with the compiler using the key; and
4 storing both correct results and plausible wrong results in an output register in
5 word locations in the output register coordinated by the key.

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1 23. The method of claim 18, further comprising:
2 providing a key shared with a compiler;
3 encrypting standard instruction op codes with the compiler using the key;
4 providing data and instruction op codes to the computer via program information
5 including an intentional introduction of errors which are correctable with error correction
6 algorithms, said correction algorithms pre-selected according to the key and long
7 instruction words; and
8 changing the correction algorithms on a periodic basis by codes hidden in the
9 instruction op codes gathered into an instruction buffer.

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1 26. Method for limiting operability of a computer program to selected ones of
2 individual microprocessors, comprising:
3 providing error correction control information for use in executing the program;
4 and
5 compiling program instruction op codes with intentionally inserted errors
6 correctable by use of said error correction control information.

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